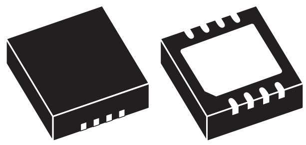
TS2007

3W filter-free Class D audio power amplifer with 6-12dB fixed gain select

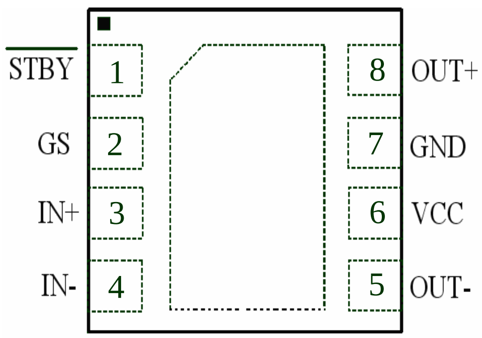
Features

- Operating range from V_{CC}=2.4V to 5.5V
- Standby mode active low
- Output power: 1.4W @5V or 0.45W @ 3.0V into 8Ω with 1% THD+N max.
- Output power: 2.3W @5V or 0.75W @ 3.0V into 4Ω with 1% THD+N max.
- Fixed gain select: 6dB or 12dB
- Low current consumption
- Efficiency: 88% typ.
- Signal-to-noise ratio: 94dB typ.
- PSRR: 63dB typ @ 217Hz with 6dB gain.
- PWM base frequency: 280kHz
- Low pop & click noise
- Thermal shutdown protection
- DFN8 3x3mm package

TS2007IQT - DFN8



TS2007IQT - DFN8



Applications

- Cellular phone
- PDA
- Notebook PC

Description

The TS2007 is a class D power audio amplifier. Able to drive up to 1.4W into an 8 Ω load at 5V, it achieves outstanding efficiency compared to typical class AB audio power amplifier.

This device allows to switch between two different gains: 6 or 12dB via a logic signal on the GS pin. A pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms. A standby function (active low) allows to lower the current consumption down to 10nA typ.

The TS2007 is available in DFN8 3x3mm lead-free packages.

Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
Pd	Power dissipation	Internally limited(4)	
ESD	HBM: human body model	2	kV
ESD	MM: machine model	200	V
Latch-up	Latch-up immunity	Class A	
	Lead temperature (soldering, 10sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of the input signal must never exceed V_{CC} + 0.3V / GND - 0.3V.
3. The device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4. Exceeding the power derating curves during a long period will cause abnormal operation.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.4 to 5.5	V
V_I	Input voltage range	GND to V_{CC}	V
V_{ic}	Input common mode voltage(1)	GND+0.15V to V_{CC}-0.7V	V
V_{STBY}	Standby voltage input (2) Device ON Device OFF	 $1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$ (3)	V
GS	Gain select input: Gain =12dB Gain = 6dB	 $GND \leq V_{GS} \leq 0.4$ $1.4 \leq V_{GS} \leq V_{CC}$	V
R_L	Load resistor	≥ 4	Ω
R_{thja}	Thermal resistance junction to ambient (4)	40	°C/W

1. I V_{oo} I $\leq$ 35mV max with both differential gains.
2. Without any signal on V_{STBY}, the device is in standby (internal 300kΩ pull down resistor).
3. Minimum current consumption is obtained when V_{STBY} = GND.
4. When mounted on 4-layer PCB.

2 Typical application

Figure 1. Typical application schematics

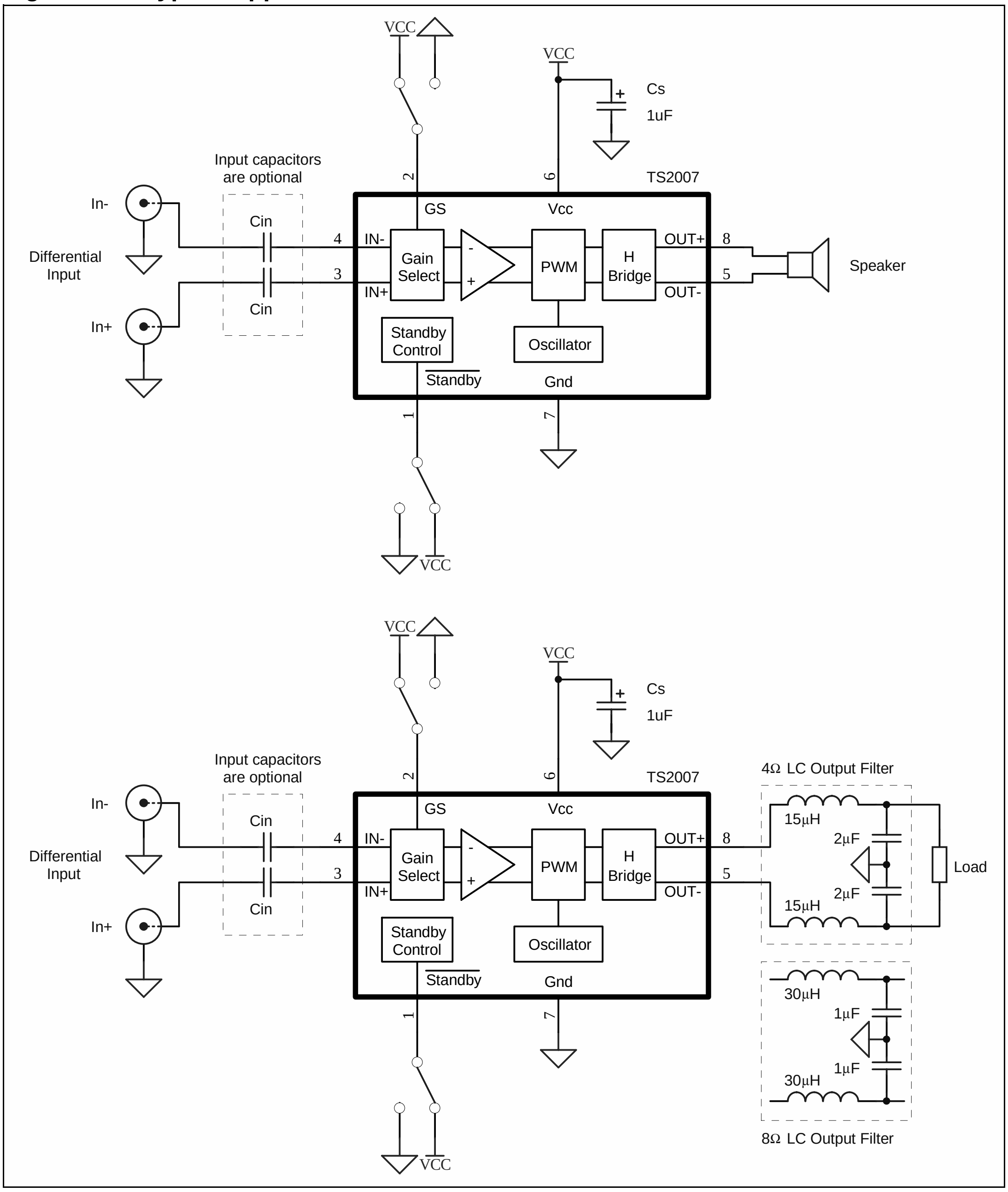


Table 3. External component descriptions

Components	Functional description
C_S	Supply capacitor that provides power supply filtering.
C_{in}	Input coupling capacitors (optional) that block the DC voltage at the amplifier input terminal. The capacitors also form a high pass filter with Z_{in} ($F_{cl} = 1 / (2 \times Pi \times Z_{in} \times C_{in})$).

Table 4. Pin descriptions

Pin number	Pin name	Pin description
1	STBY	Standby pin (active low)
2	GS	Gain select input
3	IN+	Positive differential input
4	IN-	Negative differential input
5	OUT-	Negative differential output
6	VCC	Power supply
7	GND	Ground
8	OUT+	Positive differential output

3 Electrical characteristics

3.1 Electrical characteristic tables

Table 5. V_{CC} = +5V, GND = 0V, V_{ic}=2.5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2.3	3.3	mA
$I_{CC\text{-}STBY}$	Standby current (1) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, R_L = 8Ω			25	mV
P_o	Output power THD = 1% max, f = 1kHz, R_L = 4Ω THD = 1% max, f = 1kHz, R_L = 8Ω THD = 10% max, f = 1kHz, R_L = 4Ω THD = 10% max, f = 1kHz, R_L = 8Ω		 2.3 1.4 2.8 1.7		W
THD + N	Total harmonic distortion + noise P_o = 1W_{RMS}, G = 6dB, f =1kHz, R_L = 8Ω		0.4		%
Efficiency	Efficiency P_o = 2.1 W_{RMS}, R_L = 4Ω (with LC output filter) P_o = 1.3 W_{RMS}, R_L = 8Ω (with LC output filter)		 84 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in}=1µF (2) f = 217Hz, R_L = 8Ω, Gain=6dB, V_{ripple} = 200mV_{pp} f = 217Hz, R_L = 8Ω, Gain=12dB, V_{ripple} = 200mV_{pp}		 63 60		dB
CMRR	Common mode rejection ratio 20Hz < f < 20kHz		60		dB
Gain	Gain value G_S =0V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	dB
Z_{in}	Single input impedance (3)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal to noise ratio (A-weighting) Po=1.5W, R_L=4Ω (with LC output filter)		94		dB
t_{WU}	Wake-up time		5	10	ms

Table 5. V_{CC} = +5V, GND = 0V, V_{ic}=2.5V, T_{amb} = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20Hz to 20kHz, R_L=4Ω Unweighted (Filterless, G=6dB) A-weighted (Filterless, G=6dB) Unweighted (with LC output filter, G=6dB) A-weighted (with LC output filter, G=6dB) Unweighted (Filterless, G=12dB) A-weighted (Filterless, G=12dB) Unweighted (with LC output filter, G=12dB) A-weighted (with LC output filter, G=12dB)		 74 50 69 49 94 65 86 64		μV_{RMS}

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217Hz.
3. Independent of Gain configuration (6 or 12dB) and between IN+ or IN- and GND.

Table 6. V_{CC} = +4.2V, GND = 0V, V_{ic}=2.1V, T_{amb} = 25°C (unless otherwise specified)(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2.1	3	mA
$I_{CC-STBY}$	Standby current (2) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, R_L = 8Ω			25	mV
P_o	Output power THD = 1% max, f = 1kHz, R_L = 4Ω THD = 1% max, f = 1kHz, R_L = 8Ω THD = 10% max, f = 1kHz, R_L = 4Ω THD = 10% max, f = 1kHz, R_L = 8Ω		1.6 0.95 1.95 1.1		W
THD + N	Total harmonic distortion + noise P_o = 800mW_{RMS}, G = 6dB, f =1kHz, R_L = 8Ω		0.45		%
Efficiency	Efficiency P_o = 1.5 W_{RMS}, R_L = 4Ω (with LC output filter) P_o = 0.95 W_{RMS}, R_L = 8Ω (with LC output filter)		85 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in}=1μF (3) f = 217Hz, R_L = 8Ω, Gain=6dB, V_{ripple} = 200mV_{pp} f = 217Hz, R_L = 8Ω, Gain=12dB, V_{ripple} = 200mV_{pp}		63 60		dB
CMRR	Common mode rejection ratio 20Hz < f < 20kHz		60		dB
Gain	Gain value G_S = 0V G_S = V_{CC}	11.5 5.5	12 6	12.5 6.5	dB
Z_{in}	Single input impedance (4)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal to noise ratio (A-weighting) Po=1.2W, R_L=4Ω (with LC output filter)		93		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20Hz to 20kHz, R_L=4Ω Unweighted (Filterless, G=6dB) A-weighted (Filterless, G=6dB) Unweighted (with LC output filter, G=6dB) A-weighted (with LC output filter, G=6dB) Unweighted (Filterless, G=12dB) A-weighted (Filterless, G=12dB) Unweighted (with LC output filter, G=12dB) A-weighted (with LC output filter, G=12dB)		72 50 68 49 93 65 85 64		μV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.4V and 5V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217Hz.
4. Independent of Gain configuration (6 or 12dB) and between IN+ or IN- and GND.

Table 7. V_{CC} = +3.6V, GND = 0V, V_{ic}=1.8V, T_{amb} = 25°C (unless otherwise specified)(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2	2.8	mA
$I_{CC-STBY}$	Standby current (2) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, $R_L = 8\Omega$			25	mV
P_o	Output power THD+N = 1% max, f = 1kHz, $R_L = 4\Omega$ THD+N = 1% max, f = 1kHz, $R_L = 8\Omega$ THD = 10% max, f = 1kHz, $R_L = 4\Omega$ THD = 10% max, f = 1kHz, $R_L = 8\Omega$		1.1 0.65 1.4 0.85		W
THD + N	Total harmonic distortion + noise $P_o = 500mW_{RMS}$, G = 6dB, f = 1kHz, $R_L = 8\Omega$		0.3		%
Efficiency	Efficiency $P_o = 1.1\ W_{RMS}$, $R_L = 4\Omega$ (with LC output filter) $P_o = 0.65\ W_{RMS}$, $R_L = 8\Omega$ (with LC output filter)		84 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in}=1µF (3) f = 217Hz, $R_L = 8\Omega$, Gain=6dB, $V_{ripple} = 200mV_{pp}$ f = 217Hz, $R_L = 8\Omega$, Gain=12dB, $V_{ripple} = 200mV_{pp}$		63 60		dB
CMRR	Common mode rejection ratio 20Hz < f < 20kHz		60		dB
Gain	Gain value G_S = 0V $G_S = V_{CC}$	11.5 5.5	12 6	12.5 6.5	dB
Z_{in}	Single input impedance (4)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal to noise ratio (A-weighting) Po=0.9W, R_L=4Ω (with LC output filter)		92		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20Hz to 20kHz, R_L=4Ω Unweighted (Filterless, G=6dB) A-weighted (Filterless, G=6dB) Unweighted (with LC output filter, G=6dB) A-weighted (with LC output filter, G=6dB) Unweighted (Filterless, G=12dB) A-weighted (Filterless, G=12dB) Unweighted (with LC output filter, G=12dB) A-weighted (with LC output filter, G=12dB)		72 50 68 49 93 65 85 64		μV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.4V and 5V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217Hz.
4. Independent of Gain configuration (6 or 12dB) and between IN+ or IN- and GND.

Table 8. V_{CC} = +3.0V, GND = 0V, V_{ic}=1.5V, T_{amb} = 25°C (unless otherwise specified)[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.9	2.7	mA
$I_{CC-STBY}$	Standby current [2] No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, R_L = 8Ω			25	mV
P_o	Output power THD+N = 1% Max, f = 1kHz, R_L = 4Ω THD+N = 1% Max, f = 1kHz, R_L = 8Ω THD = 10% Max, f = 1kHz, R_L = 4Ω THD = 10% Max, f = 1kHz, R_L = 8Ω		 0.75 0.45 1 0.6		W
THD + N	Total harmonic distortion + noise P_o = 400mW_{RMS}, G = 6dB, f = 1kHz, R_L = 8Ω		0.5		%
Efficiency	Efficiency P_o = 0.75 W_{RMS}, R_L = 4Ω (with LC output filter) P_o = 0.45 W_{RMS}, R_L = 8Ω (with LC output filter)		 83 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in}=1µF [3] f = 217Hz, R_L = 8Ω, Gain=6dB, V_{ripple} = 200mV_{pp} f = 217Hz, R_L = 8Ω, Gain=12dB, V_{ripple} = 200mV_{pp}		 63 60		dB
CMRR	Common mode rejection ratio 20Hz < f < 20kHz		60		dB
Gain	Gain value G_S = 0V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	dB
Z_{in}	Single input impedance [4]	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal to noise ratio (A-weighting) Po=0.6W, R_L=4Ω (with LC output filter)		90		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20Hz to 20kHz, R_L=4Ω Unweighted (Filterless, G=6dB) A-weighted (Filterless, G=6dB) Unweighted (with LC output filter, G=6dB) A-weighted (with LC output filter, G=6dB) Unweighted (Filterless, G=12dB) A-weighted (Filterless, G=12dB) Unweighted (with LC output filter, G=12dB) A-weighted (with LC output filter, G=12dB)		 71 50 67 49 92 65 85 64		µV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.4V and 5V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217Hz.
4. Independent of Gain configuration (6 or 12dB) and between IN+ or IN- and GND.

Table 9. V_{CC} = +2.4V, GND = 0V, V_{ic}=1.2V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.7	2.4	mA
$I_{CC\text{-}STBY}$	Standby current (1) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage Floating inputs, R_L = 8Ω			25	mV
P_o	Output power THD+N = 1% Max, f = 1kHz, R_L = 4Ω THD+N = 1% Max, f = 1kHz, R_L = 8Ω THD = 10% Max, f = 1kHz, R_L = 4Ω THD = 10% Max, f = 1kHz, R_L = 8Ω		 0.48 0.3 0.6 0.36		W
THD + N	Total harmonic distortion + noise P_o = 200mW_{RMS}, G = 6dB, f = 1kHz, R_L = 8Ω		0.1		%
Efficiency	Efficiency P_o = 0.38 W_{RMS}, R_L = 4Ω (with LC output filter) P_o = 0.25 W_{RMS}, R_L = 8Ω (with LC output filter)		 82 90		%
PSRR	Power supply rejection ratio with inputs grounded, C_{in}=1µF (2) f = 217Hz, R_L = 8Ω, Gain=6dB, V_{ripple} = 200mV_{pp} f = 217Hz, R_L = 8Ω, Gain=12dB, V_{ripple} = 200mV_{pp}		 63 60		dB
CMRR	Common mode rejection ratio 20Hz < f < 20kHz		60		dB
Gain	Gain value G_S = 0V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	dB
Z_{in}	Single input impedance (3)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal to noise ratio (A-weighting) Po=0.4W, R_L=4Ω (with LC output filter)		88		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5		ms
V_N	Output voltage noise f = 20Hz to 20kHz, R_L=4Ω Unweighted (filterless, G=6dB) A-weighted (filterless, G=6dB) Unweighted (with LC output filter, G=6dB) A-weighted (with LC output filter, G=6dB) Unweighted (filterless, G=12dB) A-weighted (filterless, G=12dB) Unweighted (with LC output filter, G=12dB) A-weighted (with LC output filter, G=12dB)		 70 50 66 49 91 65 84 64		µV_{RMS}

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217Hz.
3. Independent of Gain configuration (6 or 12dB) and between IN+ or IN- and GND.

3.2 Electrical characteristic curves

The graphs shown in this section use the following abbreviations:

- R_L+ 15µH or 30µH = pure resistor + very low series resistance inductor
- Filter = LC output filter (1µF+30µH for 4Ω and 0.5µF+60µH for 8Ω)

All measurements are done with C_{S1}=1µF and C_{S2}=100nF (see *Figure 2*, except for the PSRR where C_{S1} is removed (see *Figure 3*).

Figure 2. Test diagram for measurements

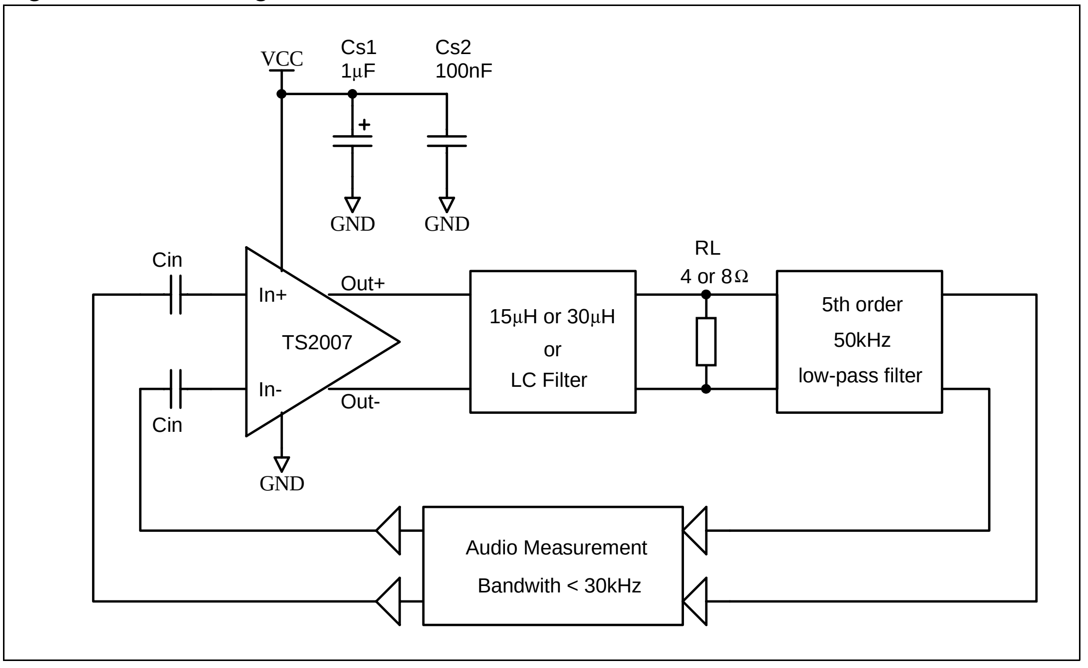


Figure 3. Test diagram for PSRR measurements

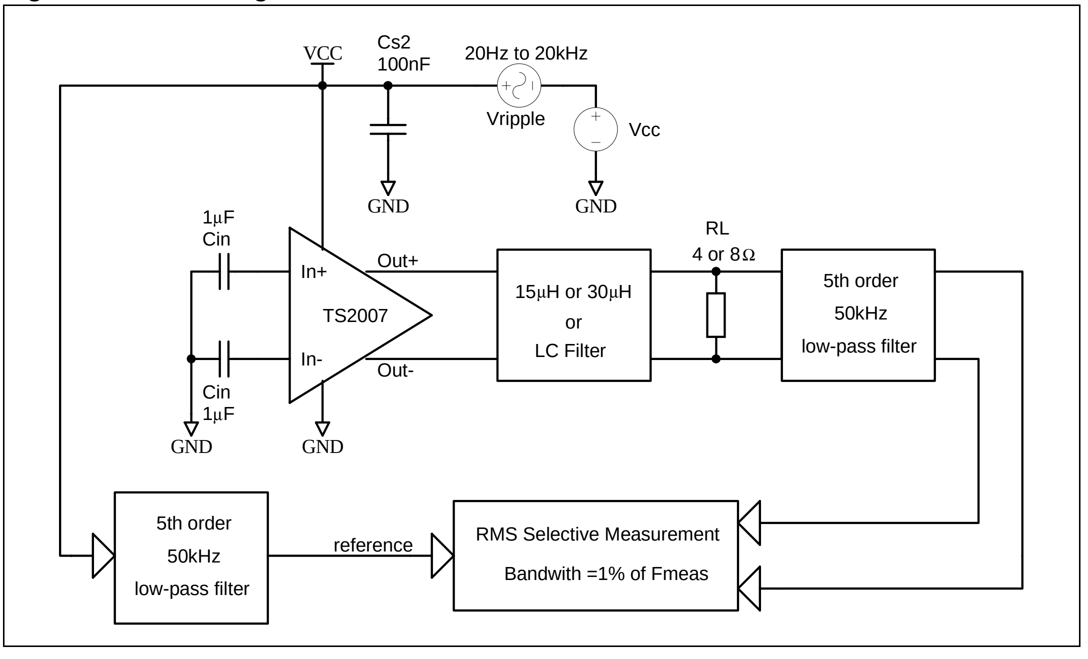


Table 10. Index of graphics

Description	Figure
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Efficiency vs. output power	*Figure 6* - *Figure 9*
Output power vs. power supply voltage	*Figure 10*, *Figure 11*
PSRR vs. common mode input voltage	*Figure 12*
PSRR vs. frequency	*Figure 13* - *Figure 17*
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Figure 4. Current consumption vs. power supply voltage

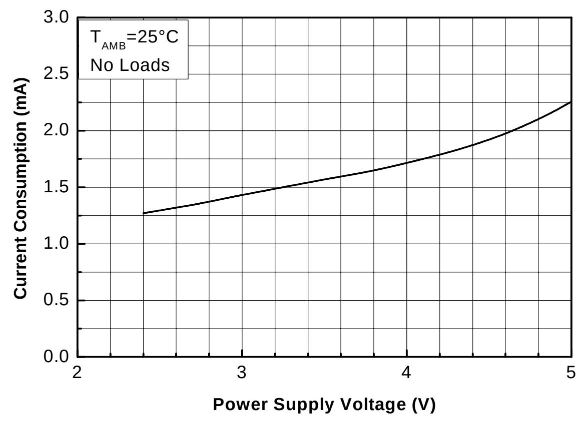


Figure 5. Current consumption vs. standby voltage

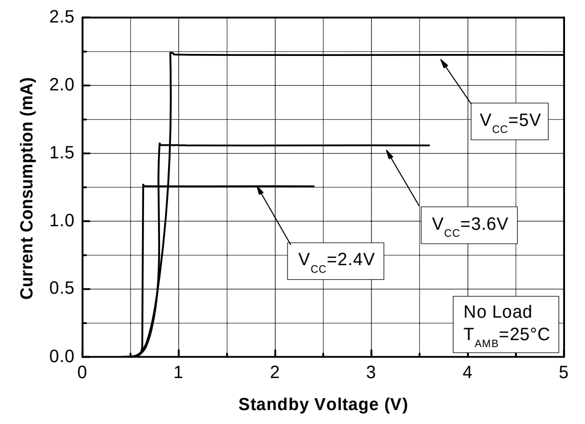


Figure 6. Efficiency vs. output power

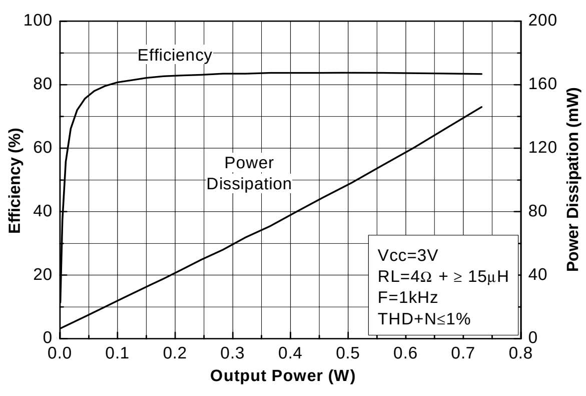


Figure 7. Efficiency vs. output power

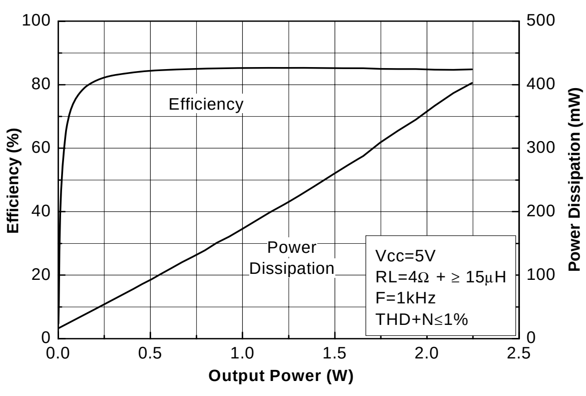


Figure 8. Efficiency vs. output power

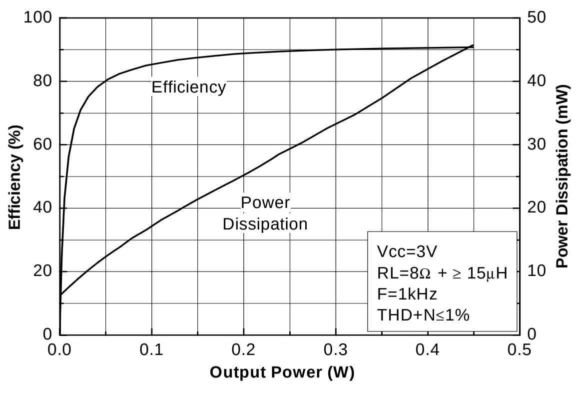


Figure 9. Efficiency vs. output power

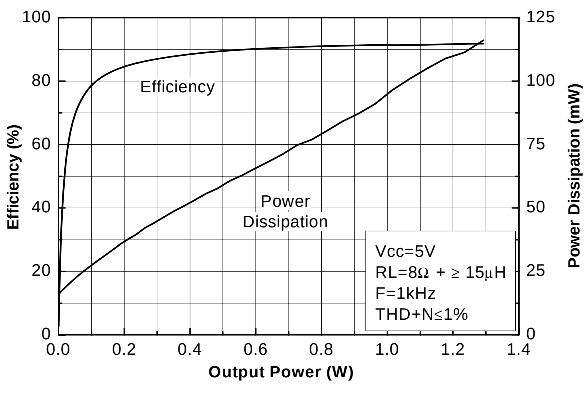


Figure 10. Output power vs. power supply voltage

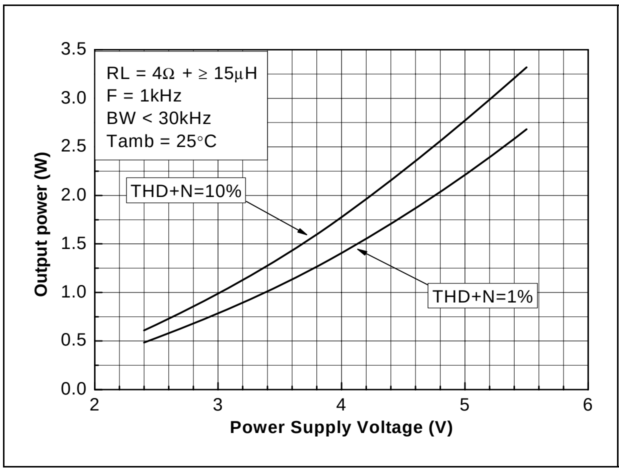


Figure 11. Output power vs. power supply voltage

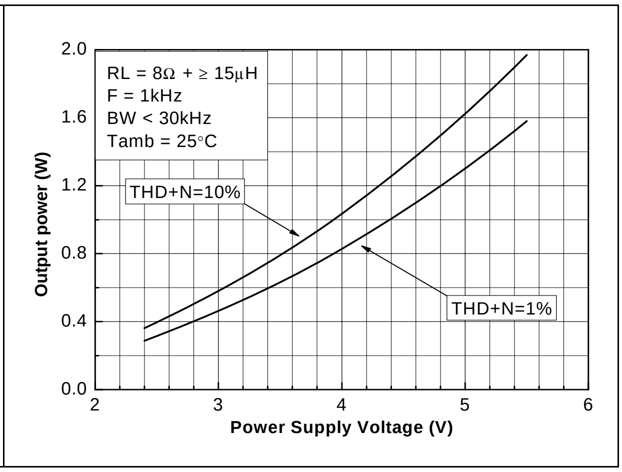


Figure 12. PSRR vs. common mode input voltage

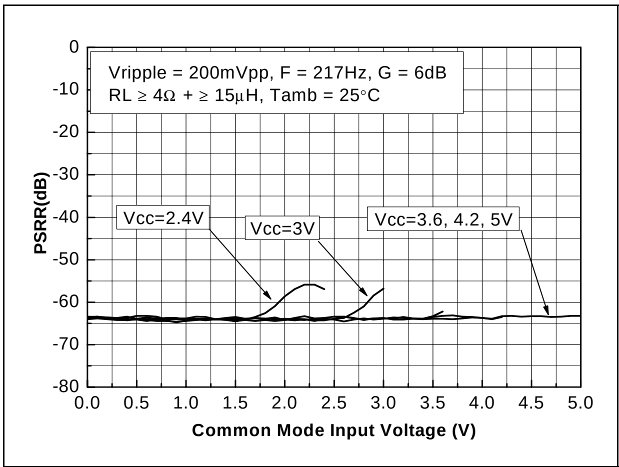


Figure 13. PSRR vs. frequency

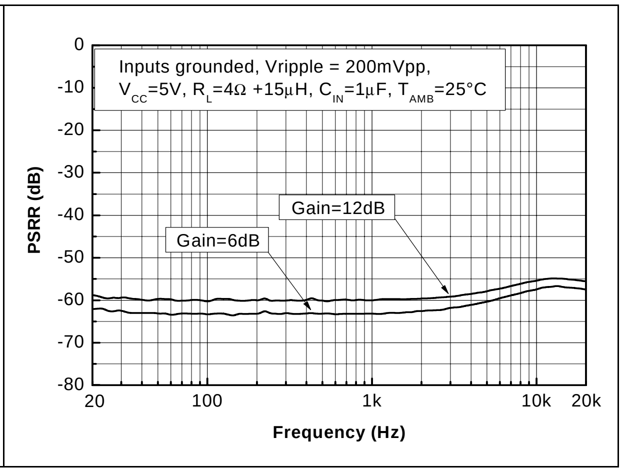


Figure 14. PSRR vs. frequency

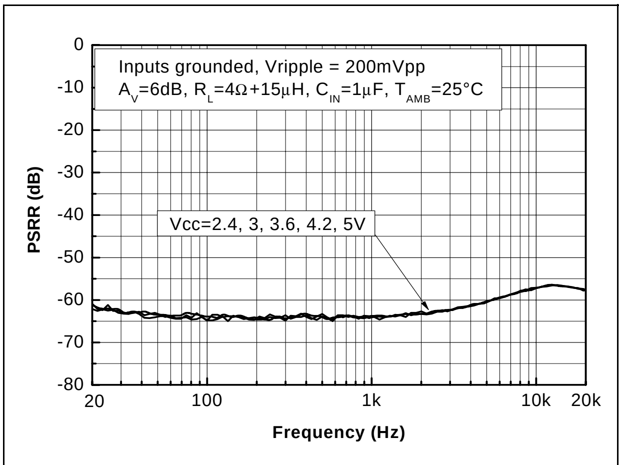


Figure 15. PSRR vs. frequency

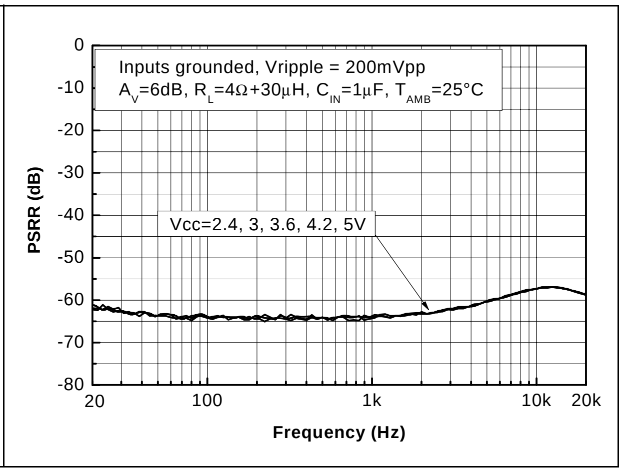


Figure 16. PSRR vs. frequency

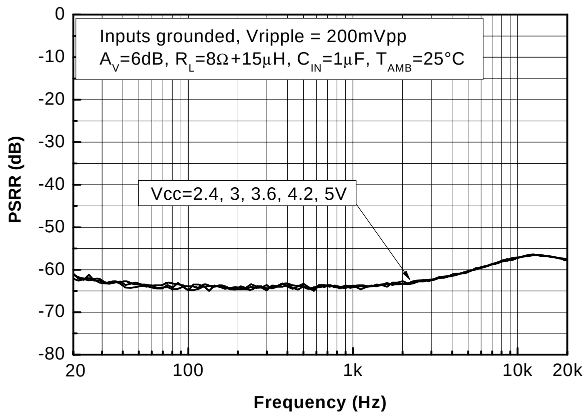


Figure 17. PSRR vs. frequency

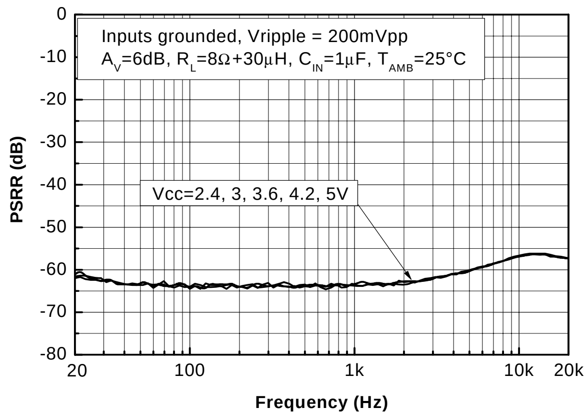


Figure 18. CMRR vs. common mode input voltage

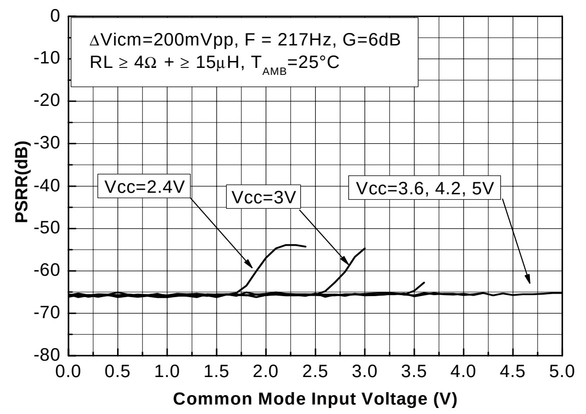


Figure 19. CMRR vs. frequency

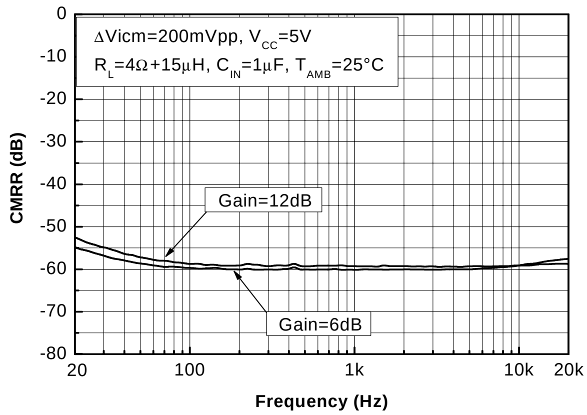


Figure 20. CMRR vs. frequency

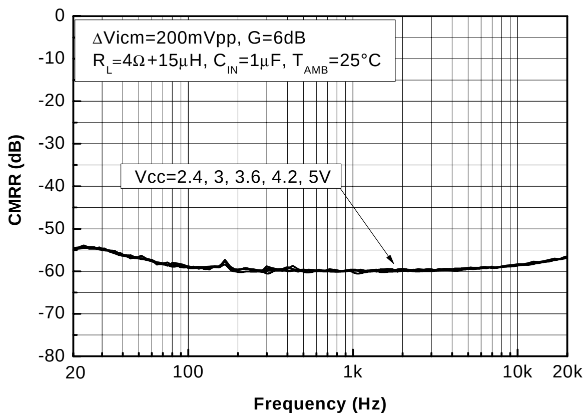


Figure 21. CMRR vs. frequency

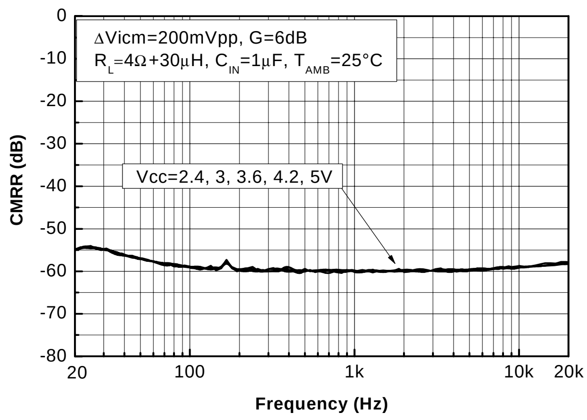


Figure 22. CMRR vs. frequency

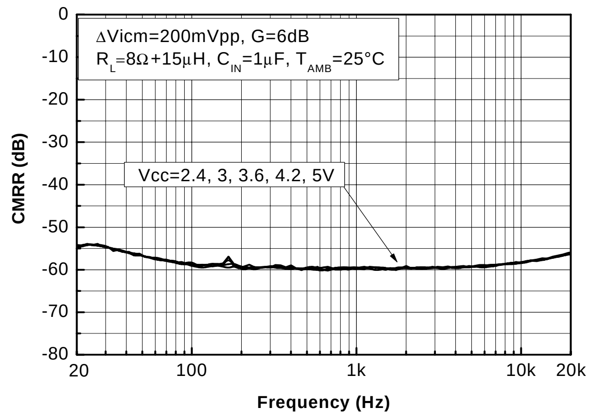


Figure 23. CMRR vs. frequency

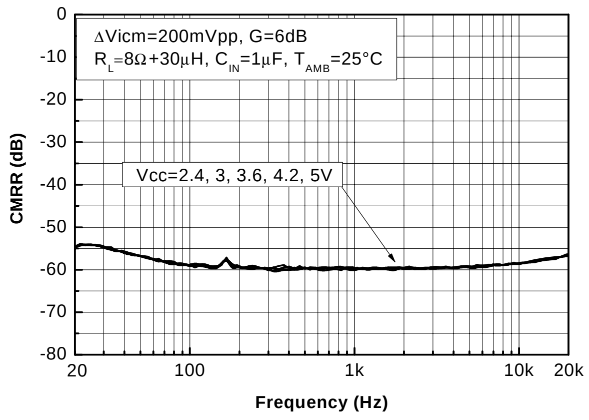


Figure 24. Gain vs. frequency

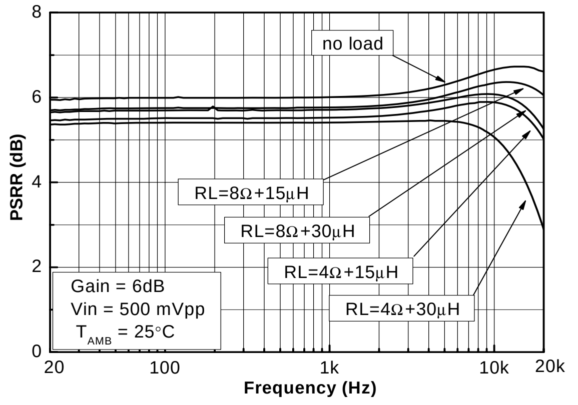


Figure 25. Gain vs. frequency

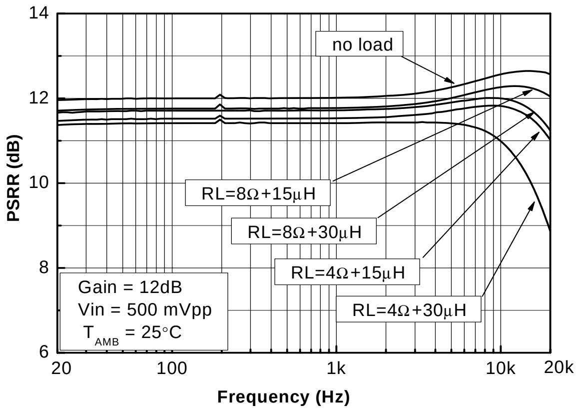


Figure 26. THD+N vs. output power

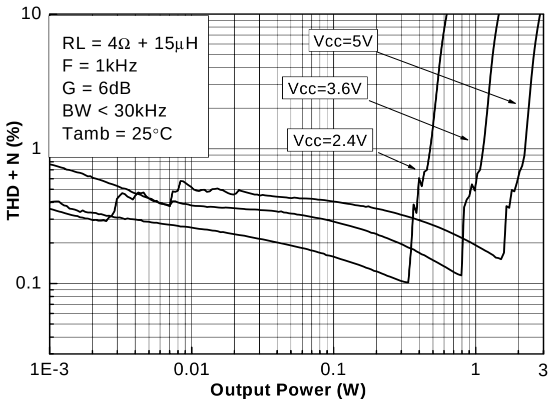


Figure 27. THD+N vs. output power

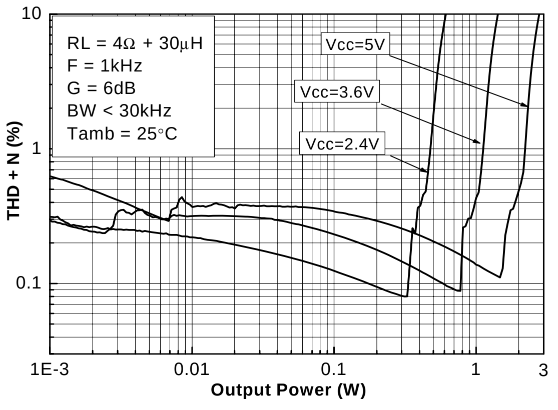


Figure 28. THD+N vs. output power

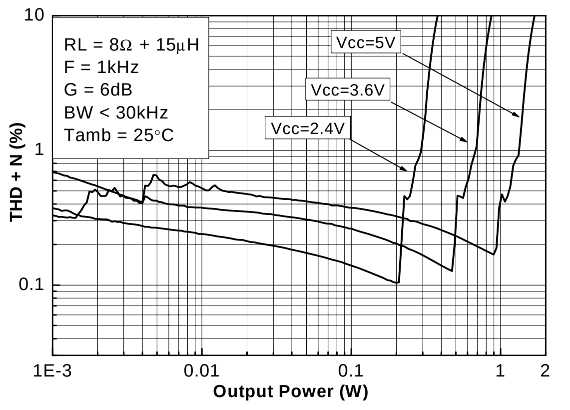


Figure 29. THD+N vs. output power

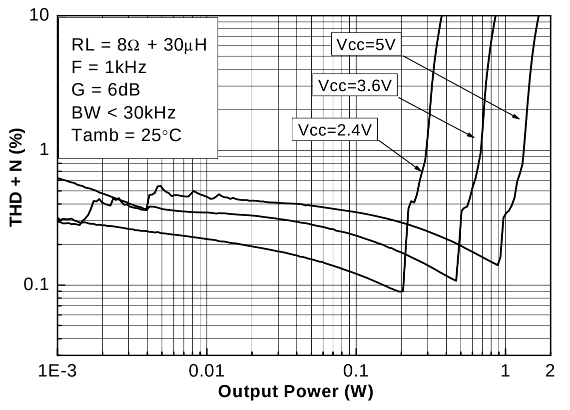


Figure 30. THD+N vs. output power

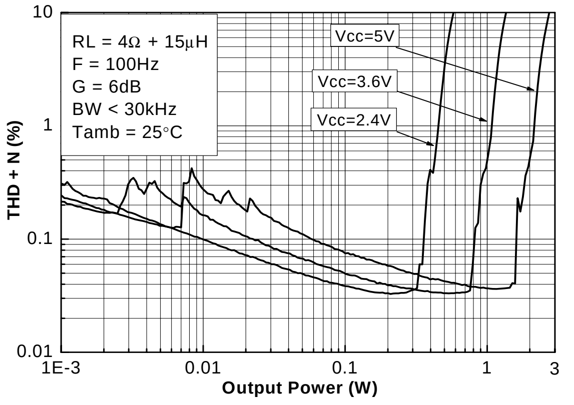


Figure 31. THD+N vs. output power

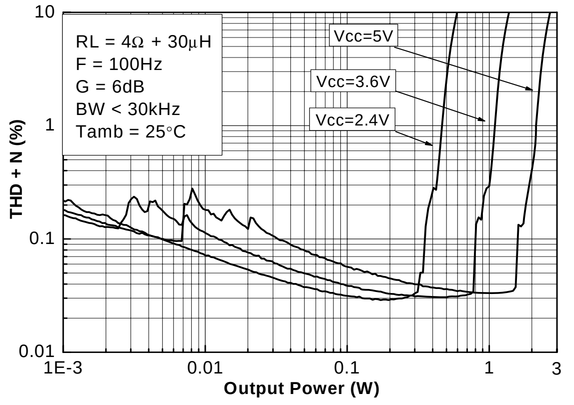


Figure 32. THD+N vs. output power

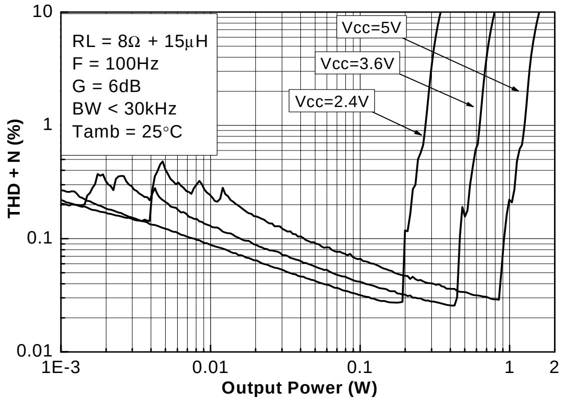


Figure 33. THD+N vs. output power

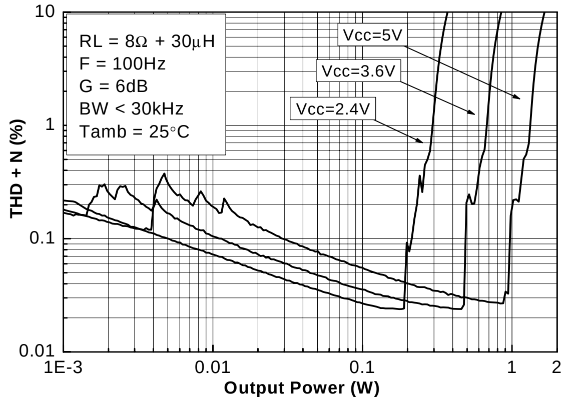


Figure 34. THD+N vs. frequency

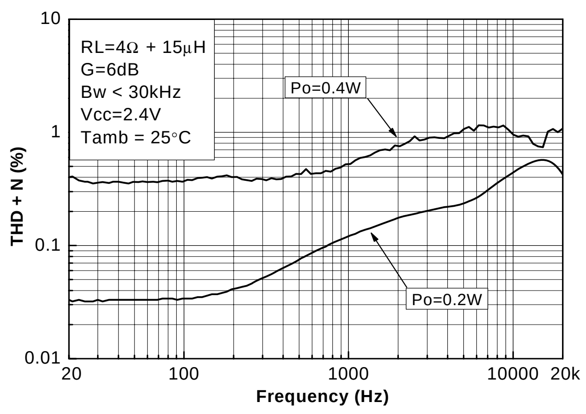


Figure 35. THD+N vs. frequency

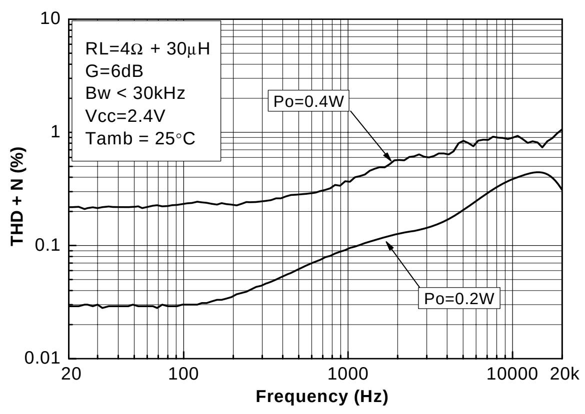


Figure 36. THD+N vs. frequency

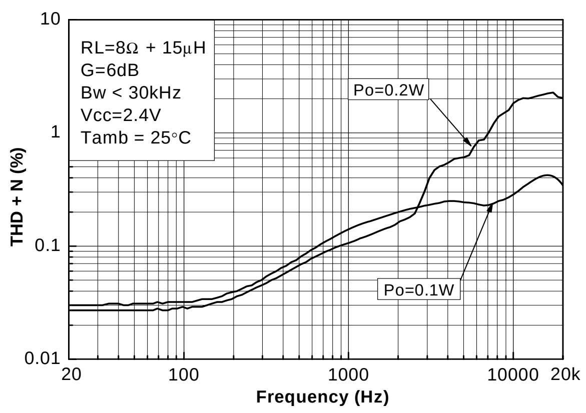


Figure 37. THD+N vs. frequency

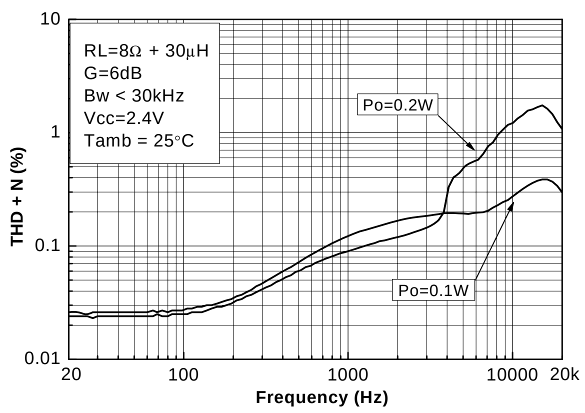


Figure 38. THD+N vs. frequency

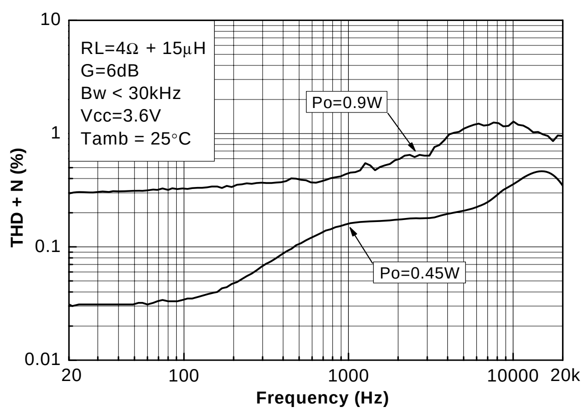


Figure 39. THD+N vs. frequency

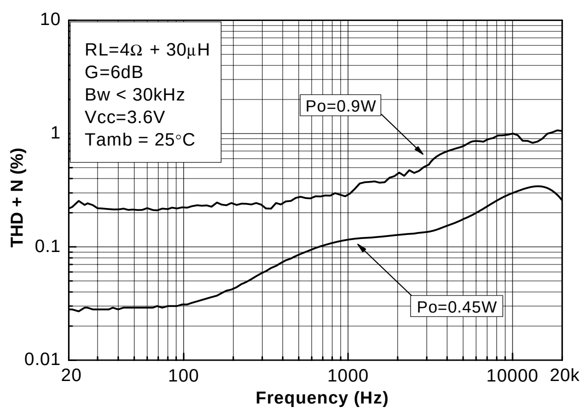


Figure 40. THD+N vs. frequency

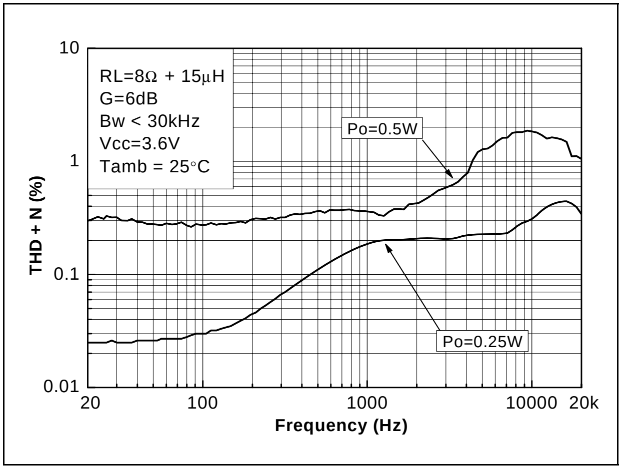


Figure 41. THD+N vs. frequency

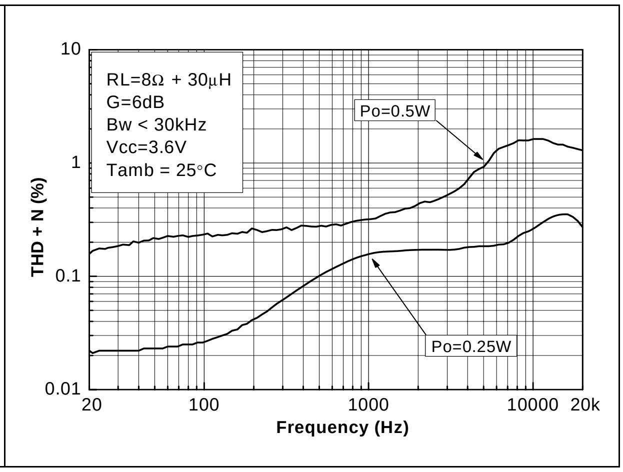


Figure 42. THD+N vs. frequency

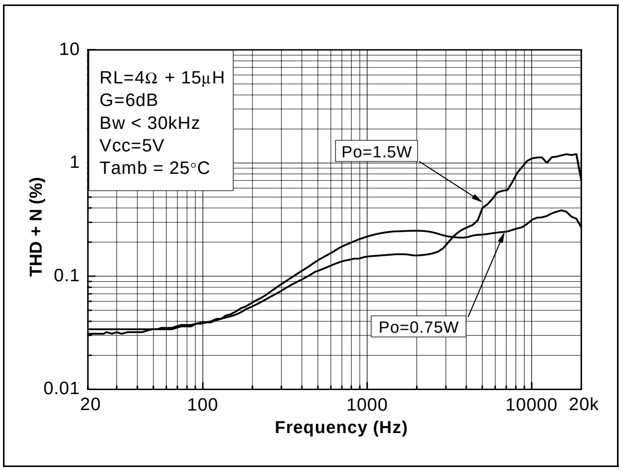


Figure 43. THD+N vs. frequency

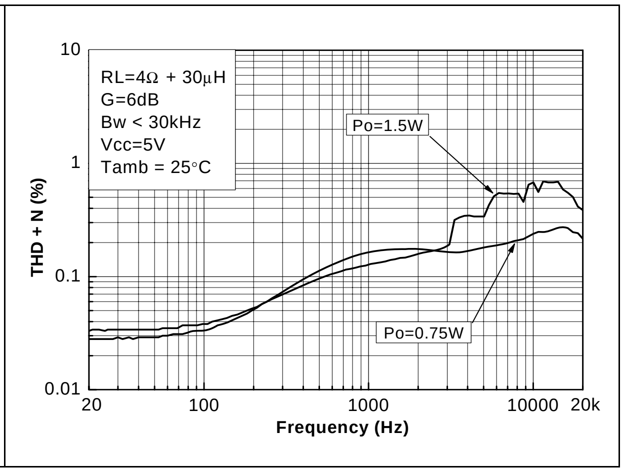


Figure 44. THD+N vs. frequency

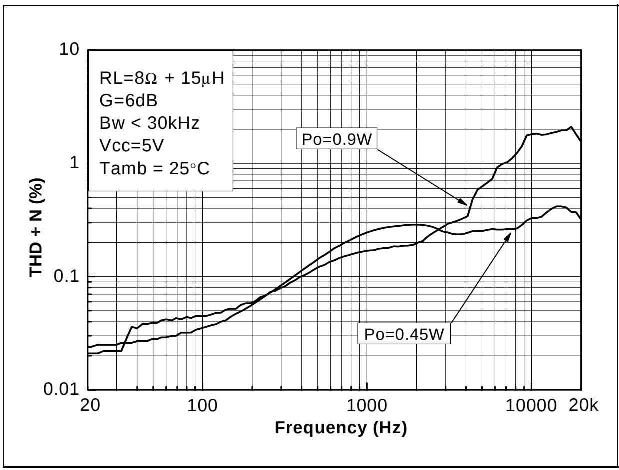


Figure 45. THD+N vs. frequency

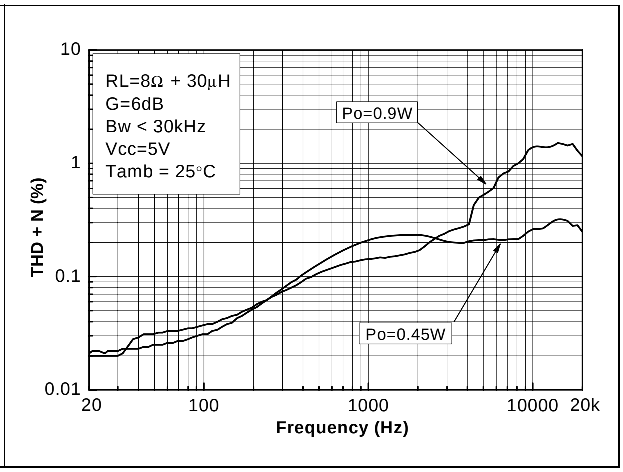


Figure 46. Power derating curves

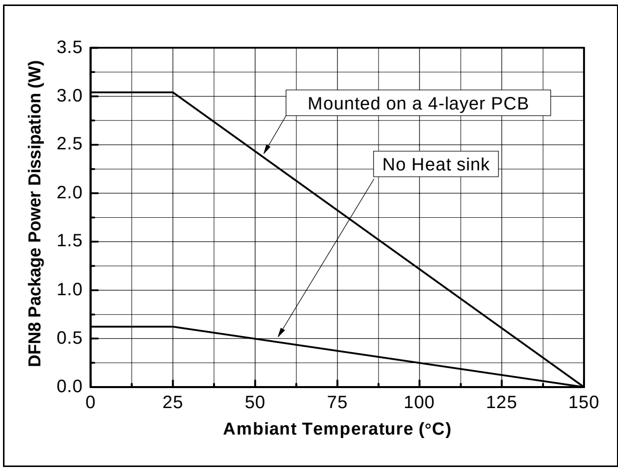


Figure 47. Startup and shutdown phase V_{CC}=5V, G=6dB, C_{in}=1µF, inputs grounded

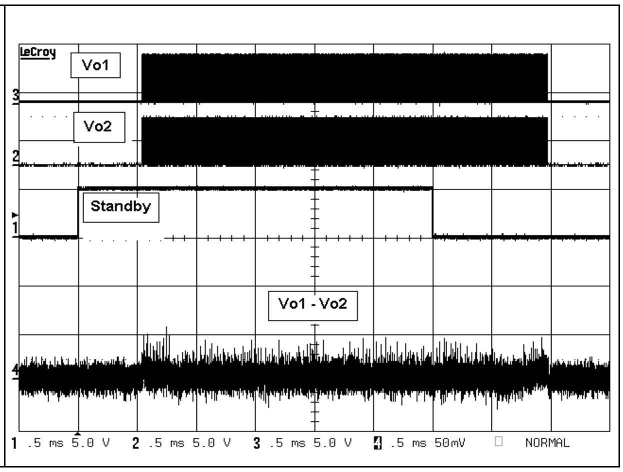


Figure 48. Startup and shutdown phase V_{CC}=5V, G=6dB, C_{in}=1µF, V_{in}=1V_{pp}, F=10kHz

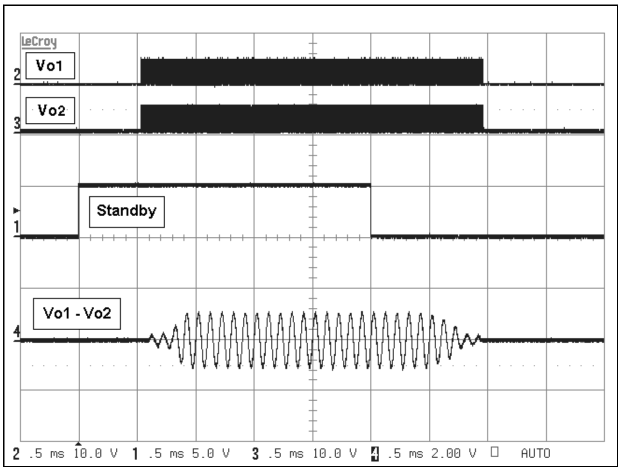
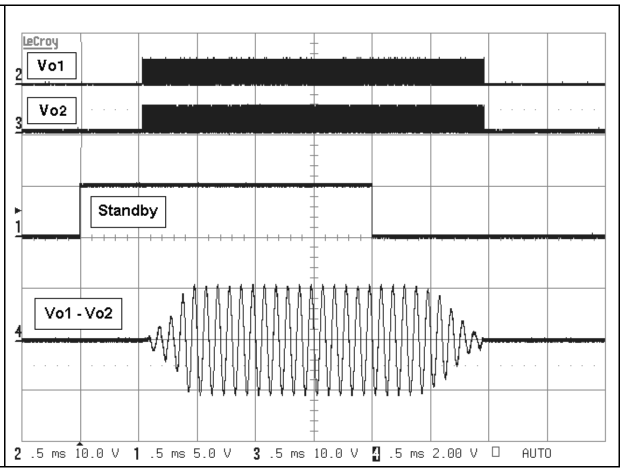


Figure 49. Startup and shutdown phase V_{CC}=5V, G=12dB, C_{in}=1µF, V_{in}=1V_{pp}, F=10kHz



4 Application information

4.1 Differential configuration principle

The TS2007 is a monolithic fully-differential input/output class D power amplifier. The TS2007 also includes a common-mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- High PSRR (power supply rejection ratio)
- High common mode noise rejection
- Virtually zero pop without additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers
- Easier interfacing with differential output audio DAC
- No input coupling capacitors required thanks to common mode feedback loop

4.2 Gain settings

In the flat region of the frequency-response curve (no input coupling capacitor or internal feedback loop + load effect), the differential gain can be set to either 6 or 12 dB depending on the logic level of the GS pin:

GS	Gain (dB)	Gain (V/V)
1	6dB	2
0	12dB	4

Note: *Between the GS pin and V_{CC} there is an internal 300kΩresistor. When the pin is floating the gain is 6 dB.*

4.3 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

Due to the V_{ic} limitation of the input stage (see *Table 2: Operating conditions on page 3*), the common mode feedback loop can fulfil its role only within the defined range.

4.4 Low frequency response

If a low frequency bandwidth limitation is required, it is possible to use input coupling capacitors. In the low frequency region, the input coupling capacitor C_{in} starts to have an effect. C_{in} forms, with the input impedance Z_{in}, a first order high-pass filter with a -3dB cut-off frequency (see *Table 5* to *Table 9*).

$$F_{CL} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot C_{in}}$$

So, for a desired cut-off frequency F_{CL} we can calculate C_{in}:

$$C_{in} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot F_{CL}}$$

with F_{CL} in Hz, Z_{in} in Ω and C_{in} in F.

The input impedance Z_{in} is for the whole power supply voltage range, typically 75kΩ. There is also a tolerance around the typical value (see *Table 5* to *Table 9*). With regard to the tolerance, you can also calculate tolerance of the F_{CL}:

- $F_{CLmax} = 1.103 \cdot F_{CL}$
- $F_{CLmin} = 0.915 \cdot F_{CL}$

4.5 Decoupling of the circuit

A power supply capacitor, referred to as C_S, is needed to correctly bypass the TS2007.

The TS2007 has a typical switching frequency of 280kHz and output fall and rise time about 5ns. Due to these very fast transients, careful decoupling is mandatory.

A 1µF ceramic capacitor is enough, but it must be located very close to the TS2007 in order to avoid any extra parasitic inductance created by a long track wire. Parasitic loop inductance, in relation with di/dt, introduces overvoltage that decreases the global efficiency of the device and may cause, if this parasitic inductance is too high, a TS2007 breakdown.

In addition, even if a ceramic capacitor has an adequate high frequency ESR value, its current capability is also important. A 0603 size is a good compromise, particularly when a 4Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1µF/6.3V capacitor used at 5V, loses about 50% of its value. With a power supply voltage of 5V, the decoupling value, instead of 1µF, could be reduced to 0.5µF. As C_S has particular influence on the THD+N in the medium to high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots which can be problematic if they reach the power supply AMR value (6V).

4.6 Wake-up time (t_{wu})

When the standby is released to set the device ON, there is a wait of 5ms typically. The TS2007 has an internal digital delay that mutes the outputs and releases them after this time in order to avoid any pop noise.

Note: The gain increases smoothly (see Figure 49) from the mute to the gain selected by the GS pin (Section 4.2).

4.7 Shutdown time

When the standby command is set, the time required to put the two output stages into high impedance and to put the internal circuitry in shutdown mode, is typically 5ms. This time is used to decrease the gain and avoid any pop noise during shutdown.

Note: The gain decreases smoothly until the outputs are muted (see Figure 49).

4.8 Consumption in shutdown mode

Between the shutdown pin and GND there is an internal 300kΩ resistor. This resistor forces the TS2007 to be in shutdown when the shutdown input is left floating.

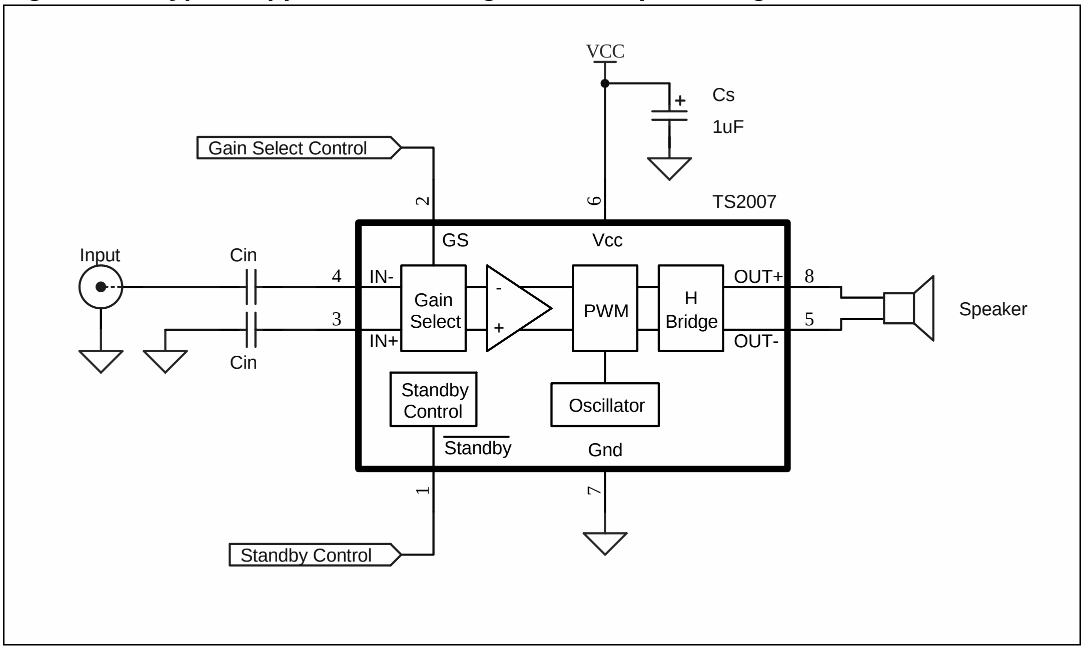
However, this resistor also introduces additional shutdown power consumption if the shutdown pin voltage is not 0V.

Referring to *Table 2: Operating conditions on page 3*, with a 0.4V shutdown voltage pin for example, you must add 0.4V/300k=1.3µA in typical (0.4V/273k=1.46µA in maximum) to the shutdown current specified in *Table 5* to *Table 9*.

4.9 Single-ended input configuration

It is possible to use the TS2007 in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The following schematic diagram shows a typical single-ended input application.

Figure 50. Typical application for single-ended input configuration



4.10 Output filter considerations

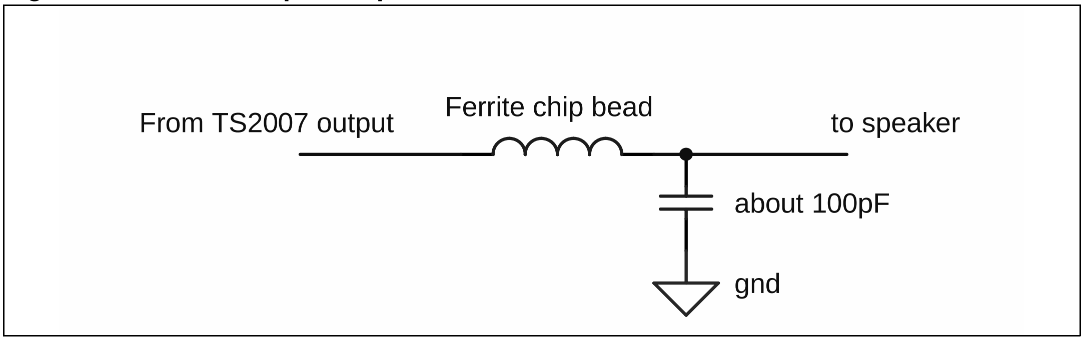
The TS2007 is designed to operate without an output filter. However, due to very sharp transients on the TS2007 output, EMI radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS2007 outputs and loudspeaker terminal are long (typically more than 50mm, or 100mm in both directions, to the speaker terminals). As the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow:

- Reduce, as much as possible, the distance between the TS2007 output pins and the speaker terminals.
- Use a ground plane for “shielding” sensitive wires.
- Place, as close as possible to the TS2007 and in series with each output, a ferrite bead with a rated current of minimum 2.5A and impedance greater than 50Ω at frequencies above 30MHz. If, after testing, these ferrite beads are not necessary, replace them by a short-circuit.
- Allow extra footprint to place, if necessary, a capacitor to short perturbations to ground (see *Figure 51*).

Figure 51. Ferrite chip bead placement



In the case where the distance between the TS2007 output and the speaker terminals is too long, it is possible to have low frequency EMI issues due to the fact that the typical operating frequency is 280kHz. In this configuration, it is necessary to use the output filter represented in *Figure 1 on page 4* as close as possible to the TS2007.

5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 52. Pinout (top view)

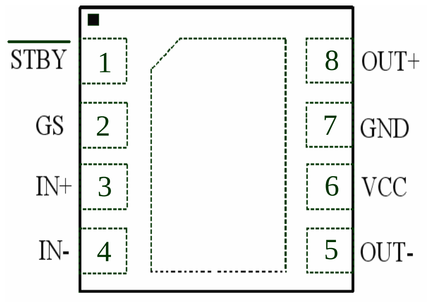


Figure 53. Marking (top view)

Logo: **ST**
Part number: **K007**
Three digit date code: **YWW**
The dot is for marking pin **1**

Figure 54. Recommended footprint for the TS2007 DFN8 package

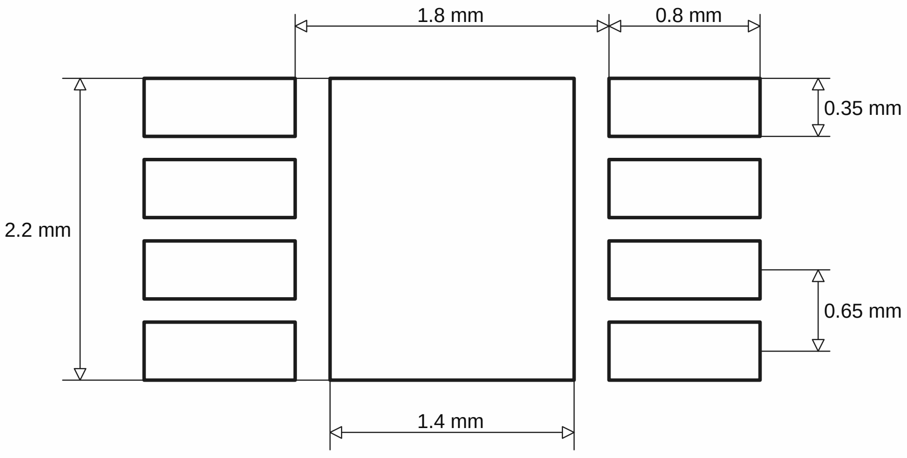
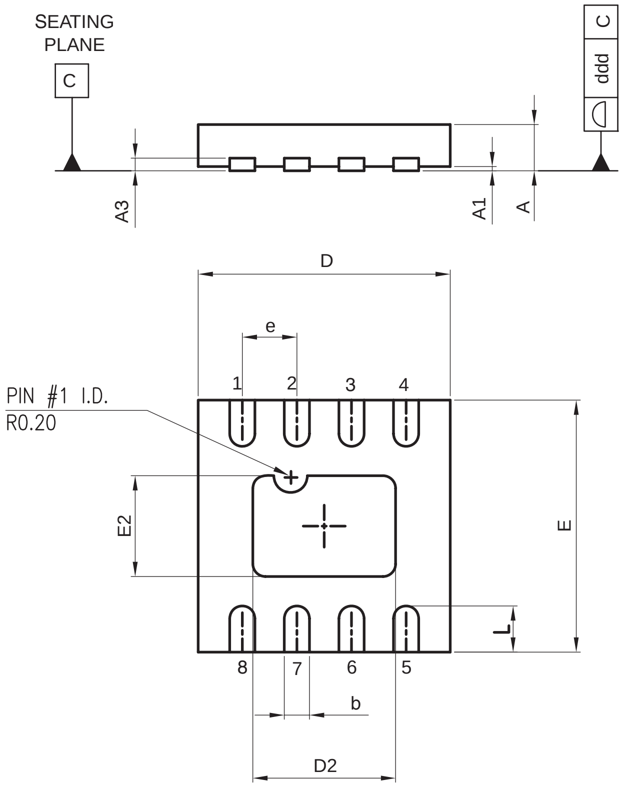


Figure 55. DFN8 package mechanical data

Ref	Dimensions					
	Millimeters			Mils		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.60	0.65	19.6	23.6	25.6
A1		0.02	0.05		0.8	1.9
A3			0.22			8.6
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.85	3.00	3.15	112.2	118.1	124
D2	1.60	1.70	1.80	63	66.9	70.8
E	2.85	3.00	3.15	112.2	118.1	124
E2	1.10	1.20	1.30	43.3	47.2	51.2
e		0.65			25.5	
L(1)	0.50	0.55	0.60	19.6	21.6	23.6
ddd			0.08			3.1



1. The dimension of L is not compliant with JEDEC MO-248 which recommends 0.40mm +/-0.10mm.

Note: The DFN8 package has an exposed pad E2 x D2. For enhanced thermal performance, the exposed pad must be soldered to a copper area on the PCB, acting as a heatsink. This copper area can be electrically connected to pin7 or left floating.

6 Ordering information

Table 11. Order code

Part number	Temperature range	Package	Marking
TS2007IQT	-40°C, +85°C	DFN8	K07

7 Revision history

Date	Revision	Changes
11-Jan-2007	1	Initial release (preliminary data).
11-May-2007	2	First complete datasheet. This release of the datasheet includes electrical characteristics curves and application information.
24-May-2007	3	Corrected error in *Table 4: Pin descriptions*: descriptions of pin 5 and pin 8 were inverted.